Performance

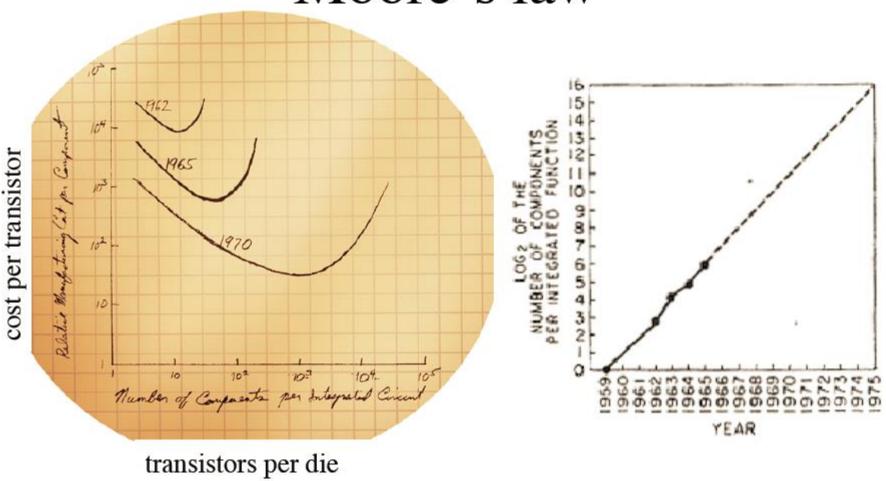
Dina Katabi & Sam Madden

6.033 Spring 2014

http://web.mit.edu/6.033

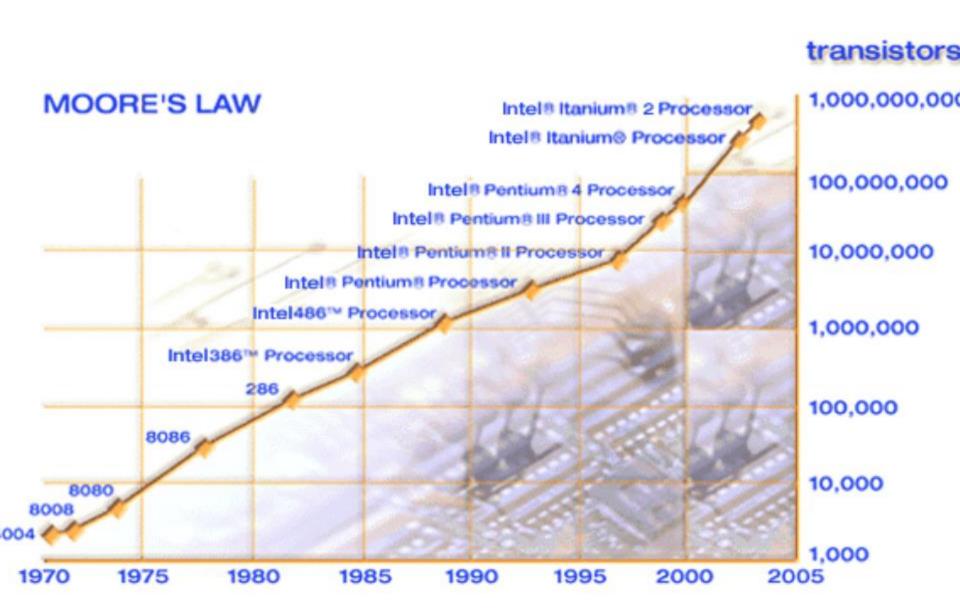


Moore's law

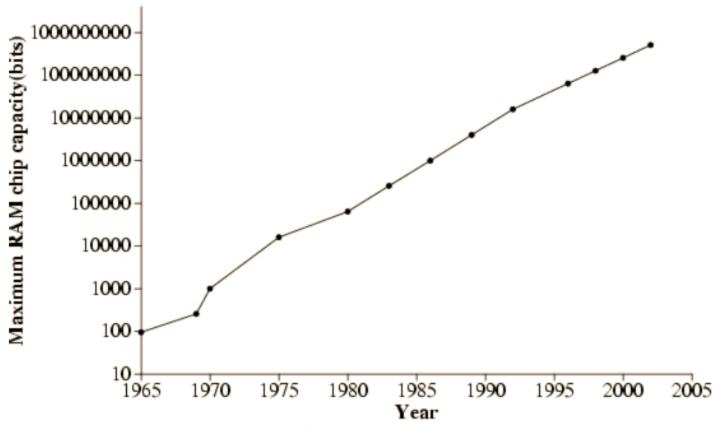


"Cramming More Components Onto Integrated Circuits", *Electronics*, April 1965

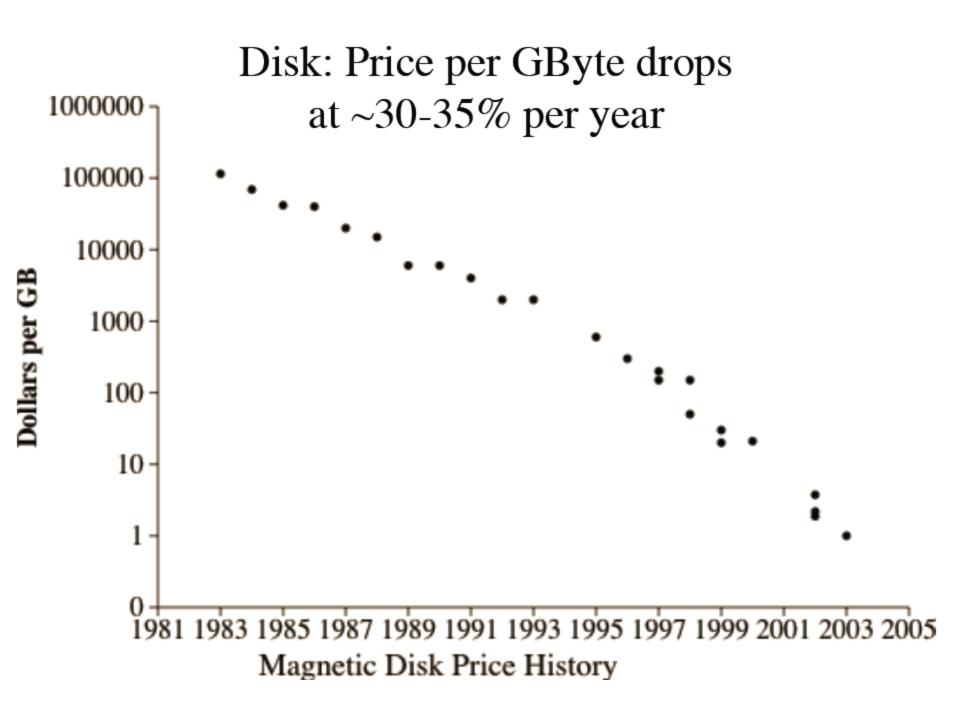
Transistors/die double every ~18 months



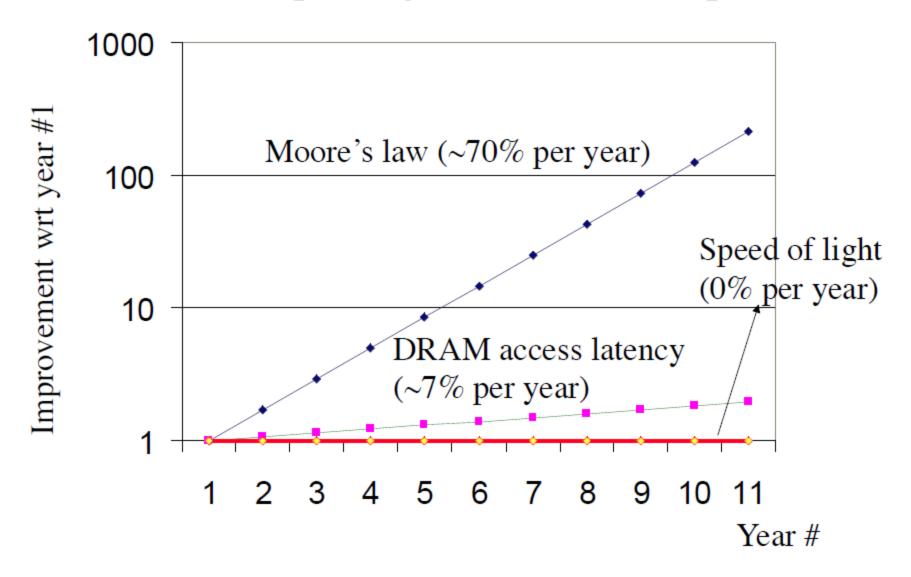
DRAM Density



Trends in semiconductor RAM density



Latency improves slowly



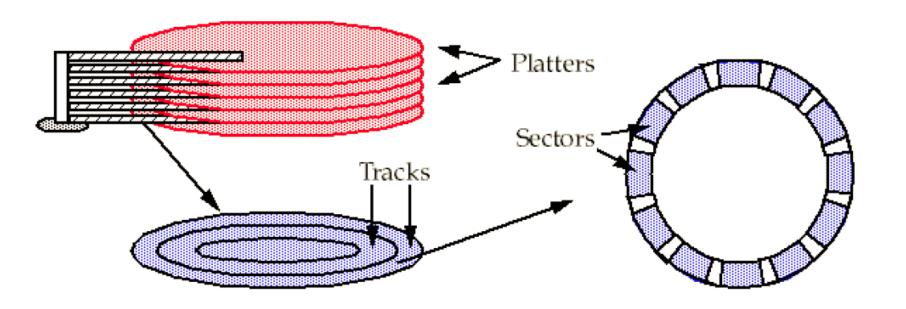
Example

```
while True:
wait for request
data = read(name)
compute
send response
```

Hitachi 7K400



Top view



88,283 tracks per platter 576 to 1170 sectors per track

Important numbers

- Latency:
 - 0.00000001 ms: instruction time (1 ns)
 - 0.0001 ms: DRAM load (100 ns)
 - 0.1 ms: LAN network
 - 10 ms: random disk I/O
 - 25 ms: Internet east -> west coast
- Throughput:
 - 10,000 MB/s: DRAM
 - 1,000 MB/s: LAN (or100 MB/s)
 - 100 MB/s: sequential disk (or 500 MB/s)
 - 1 MB/s: random disk I/O